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MS-7704

Mini-ITX Ver: 2.5

CPU:

INTEL-Sandy bridge LGA1155

System Chipset:

INTEL-Cougar Point H61

OnBoard Chipset:

HD Audio Codec:ALC892

uPD720202 USB3.0

LAN-RTL8111E

SIO:Fintek F71889AD

Flash ROM: 64 Mb SPI

Main Memory:

DDRIII (1066/1333MHz) * 2 (Dual Channel)

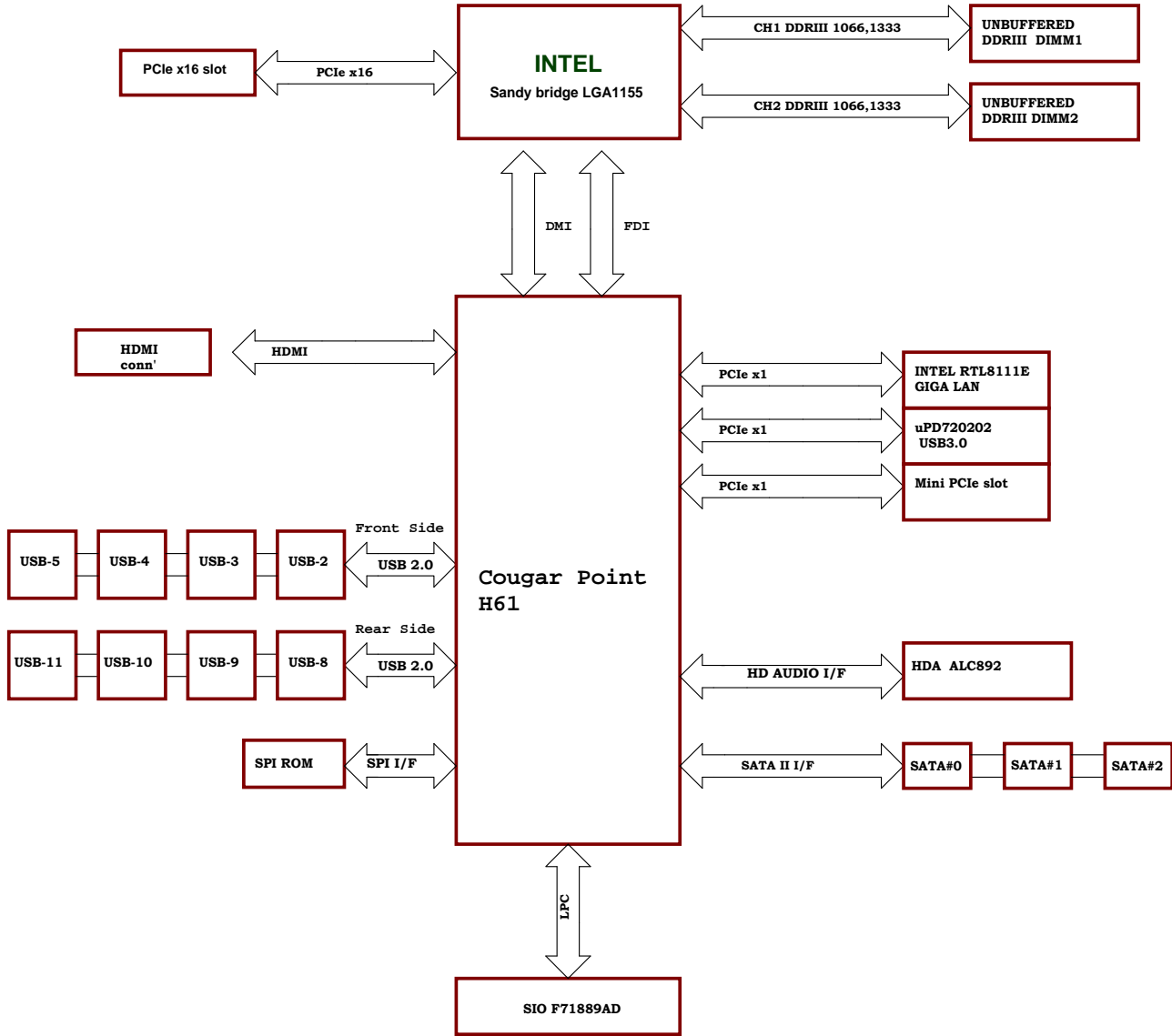
Expansion Slots:

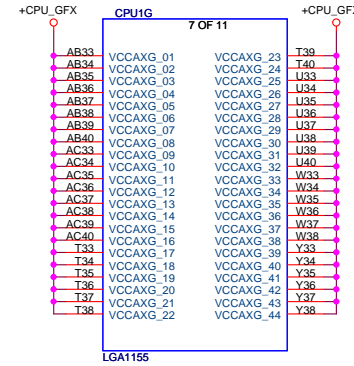
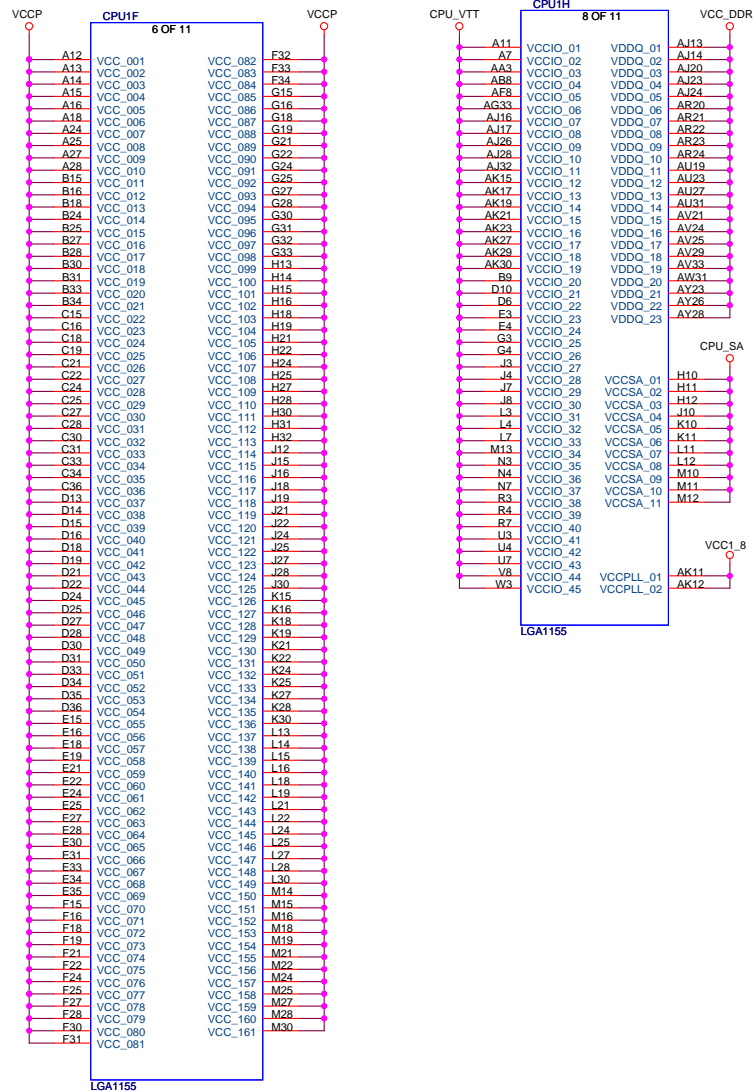
PCI Express (X16) Slot * 1

Mini PCIe(X1) Slot * 1

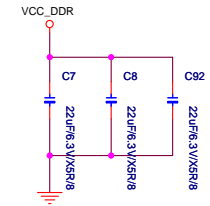
PWM:

VRD12 ISL6364 4+1 Phase Dr.MOS



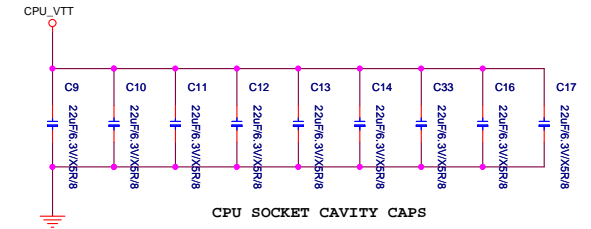


+1.5V_DDR3-Decoupling

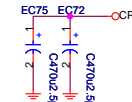


CPU SOCKET CAVITY CAPS

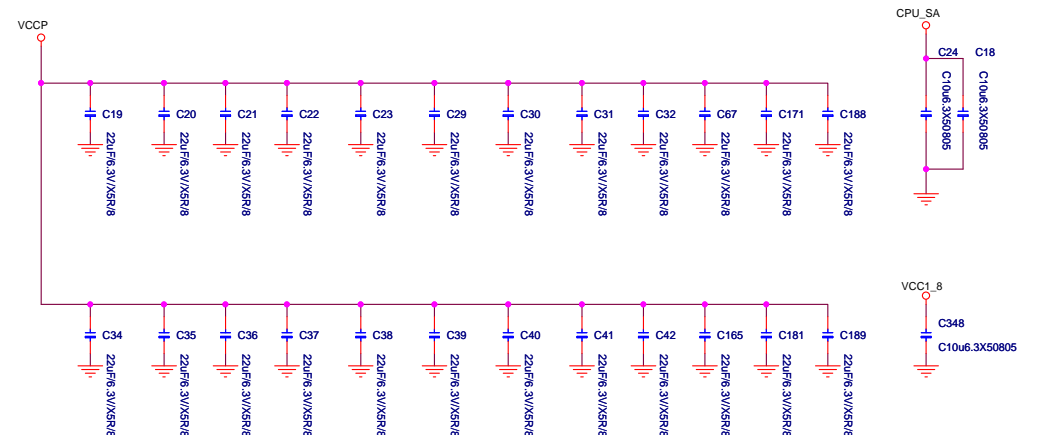
+CPU_VTT Decoupling



bottom SP Capacitors



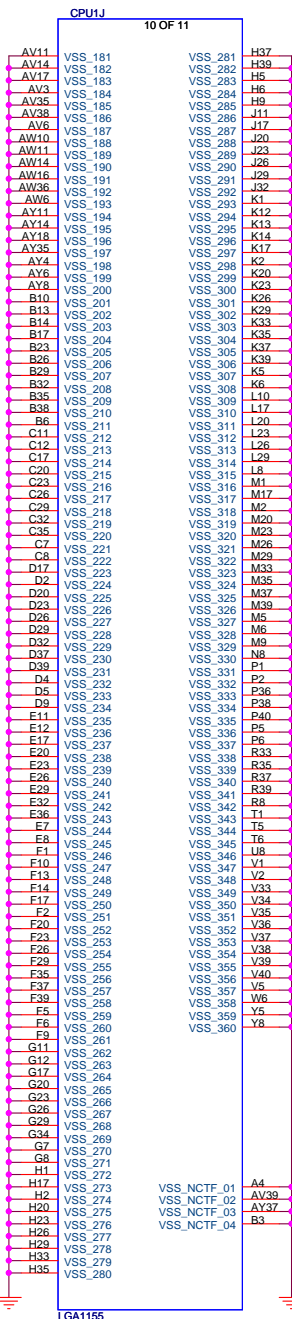
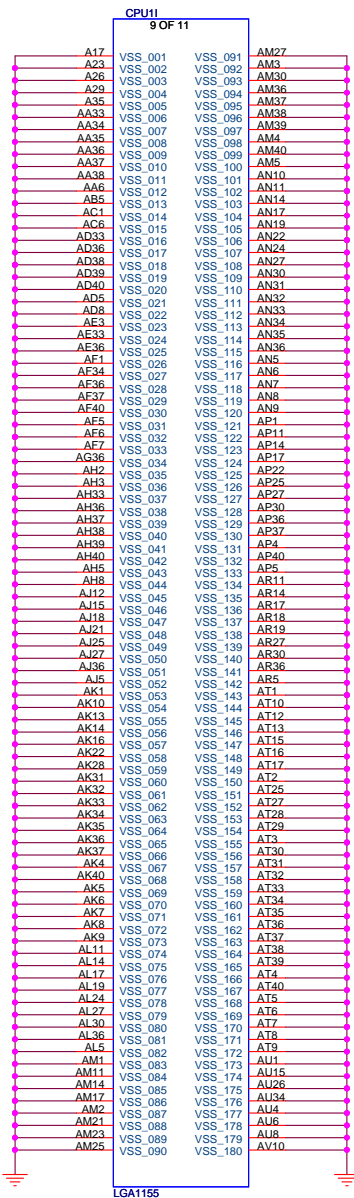
+CPU_VCCP-Decoupling



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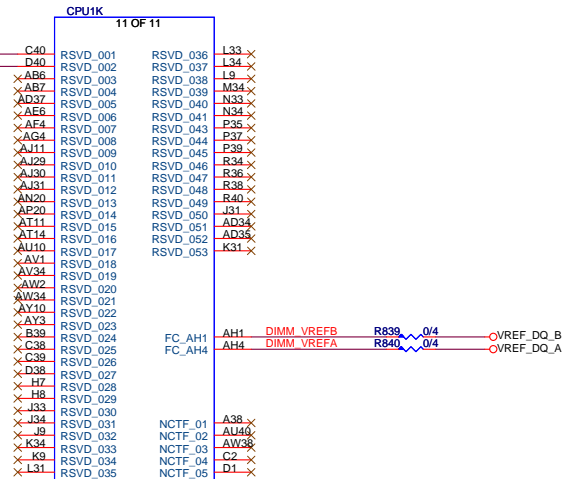
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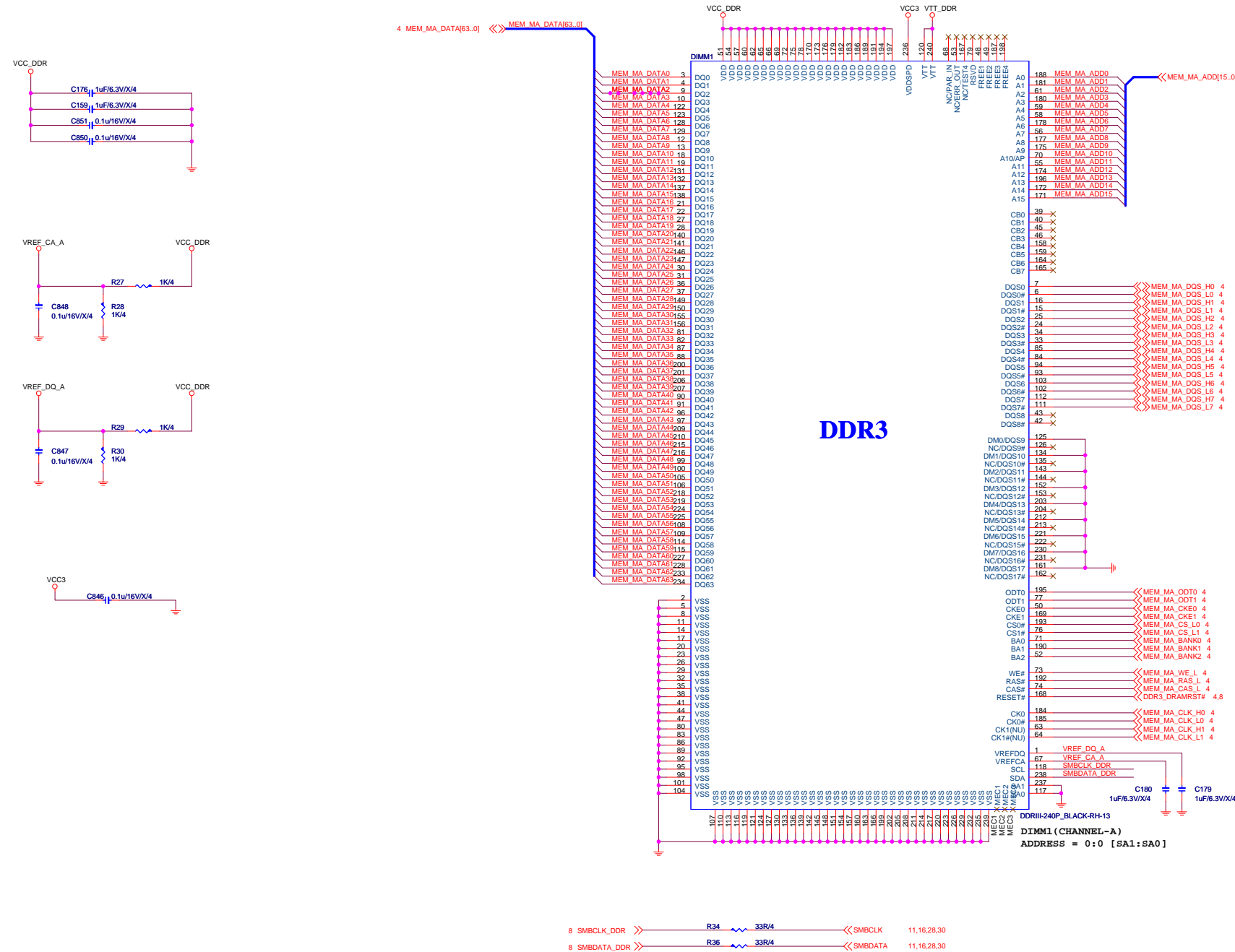
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9 XDP_CPU_BCLK_N

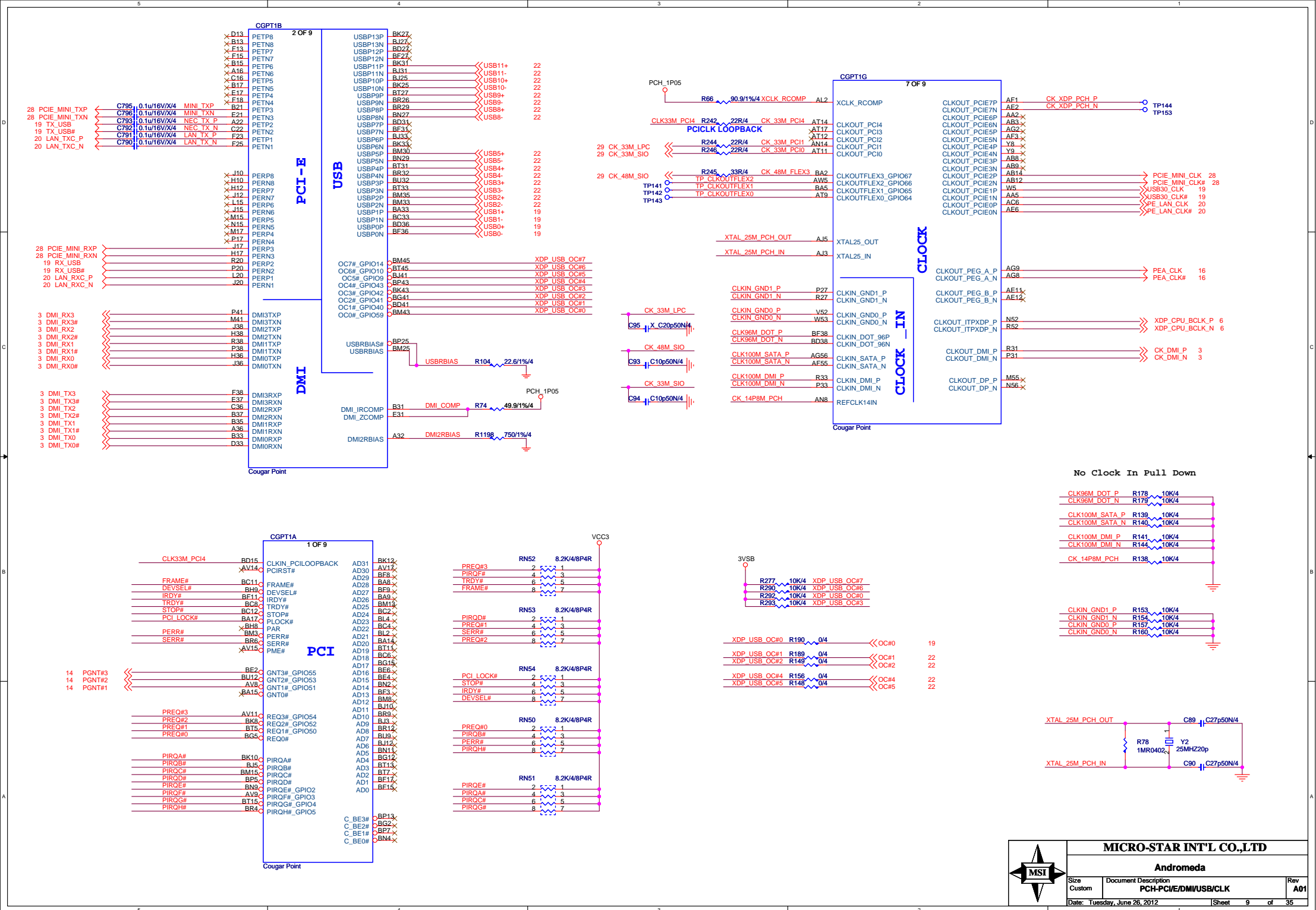
R842 X 0/4
R844 X 0/4



LGA1155

DDR3 DIMM1_A0

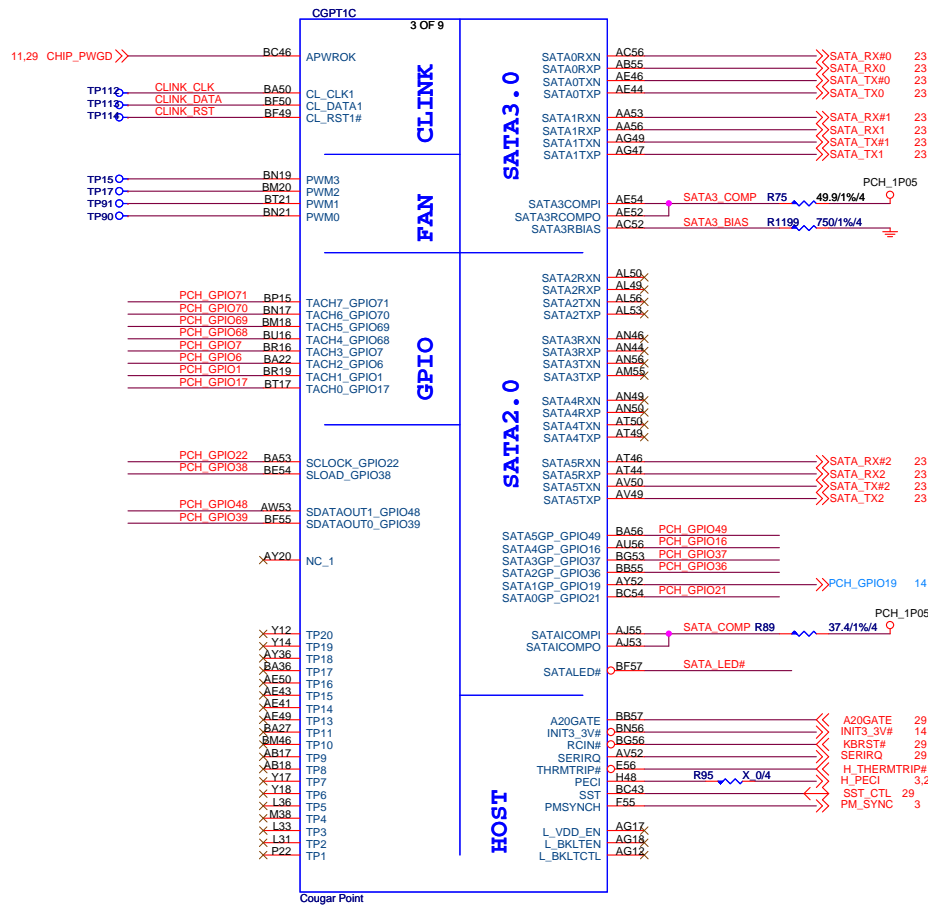




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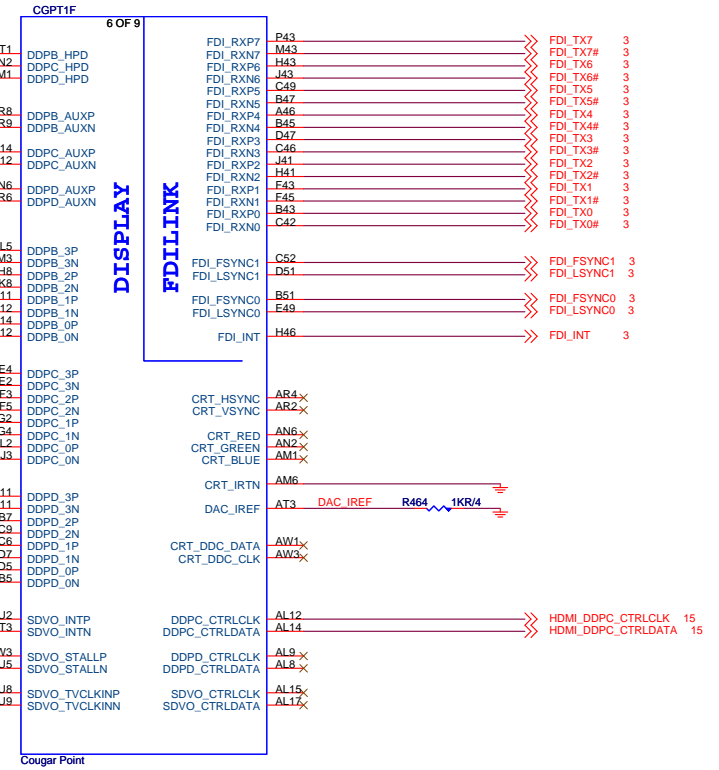
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Size Custom	Document Description PCH-PCI/E/DMI/USB/CLK	Rev A01
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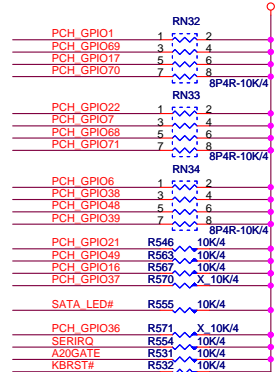


15 HDMI_DDPD_HPD >>

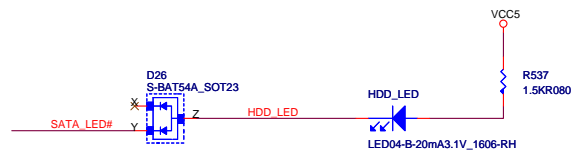
15 HDMI_DDPD_CLK_P
15 HDMI_DDPD_CLK_N
15 HDMI_DDPD_TX2_P
15 HDMI_DDPD_TX2_N
15 HDMI_DDPD_TX1_P
15 HDMI_DDPD_TX1_N
15 HDMI_DDPD_TX0_P
15 HDMI_DDPD_TX0_N



Pull HIGH for PCH



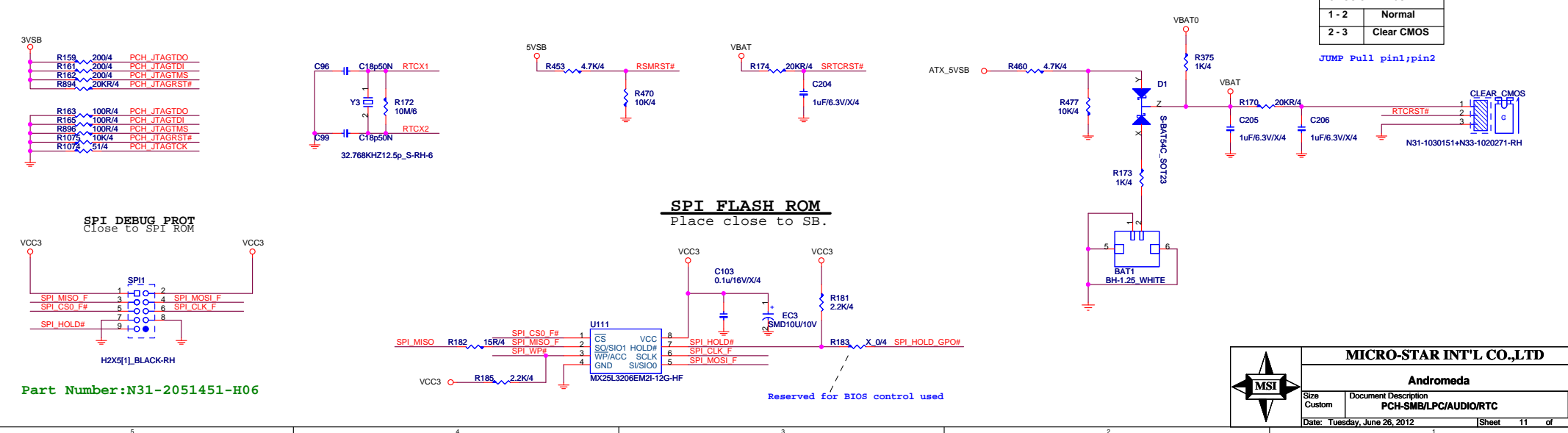
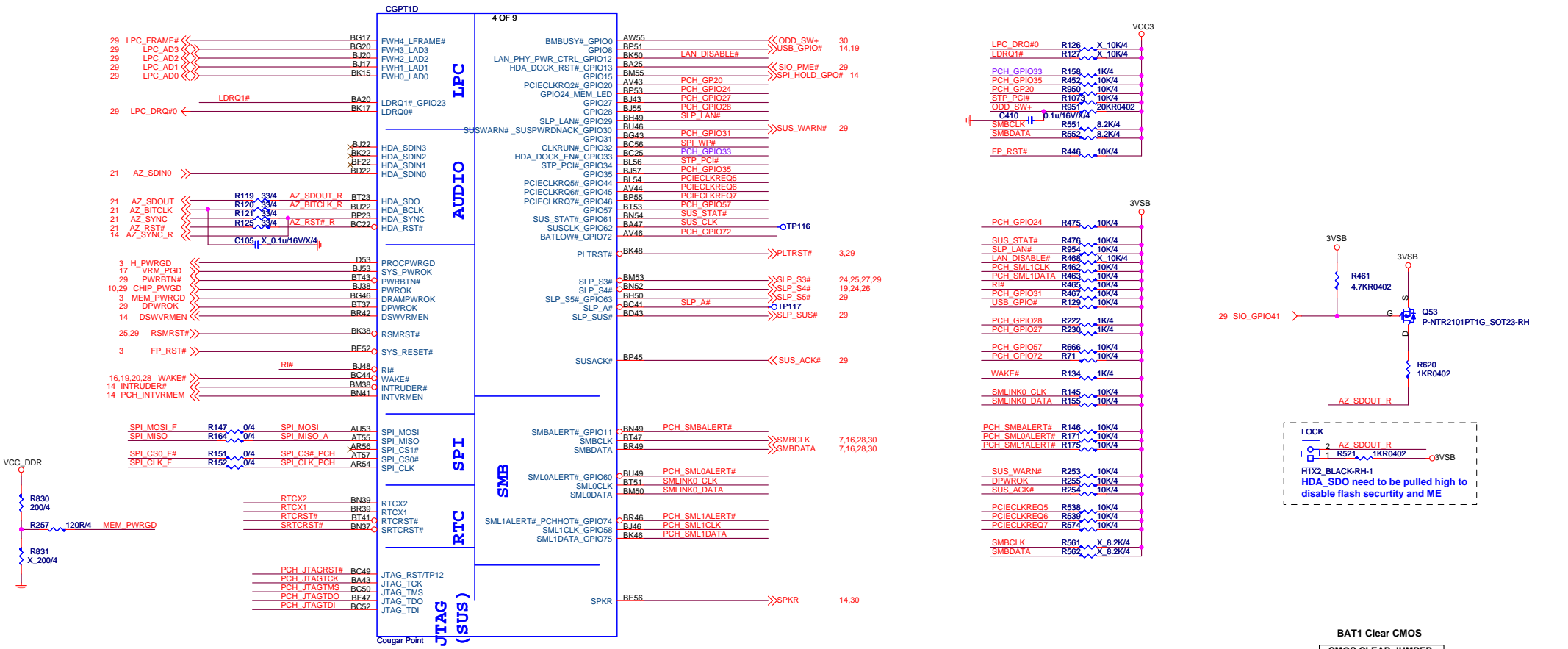
HDD LED



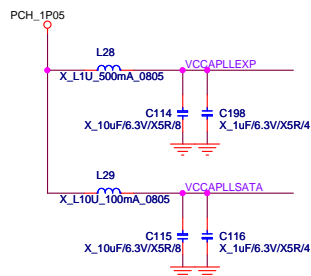
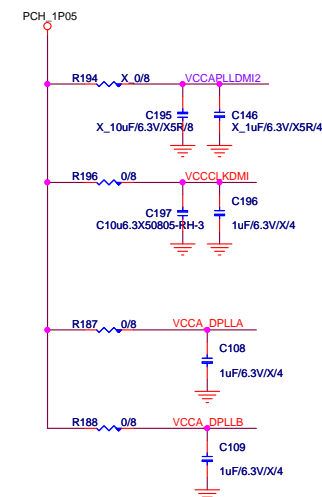
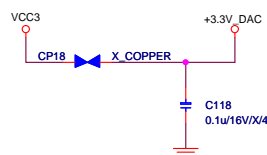
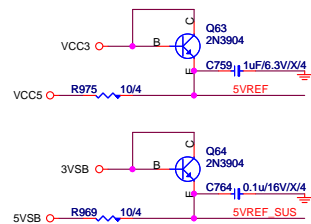
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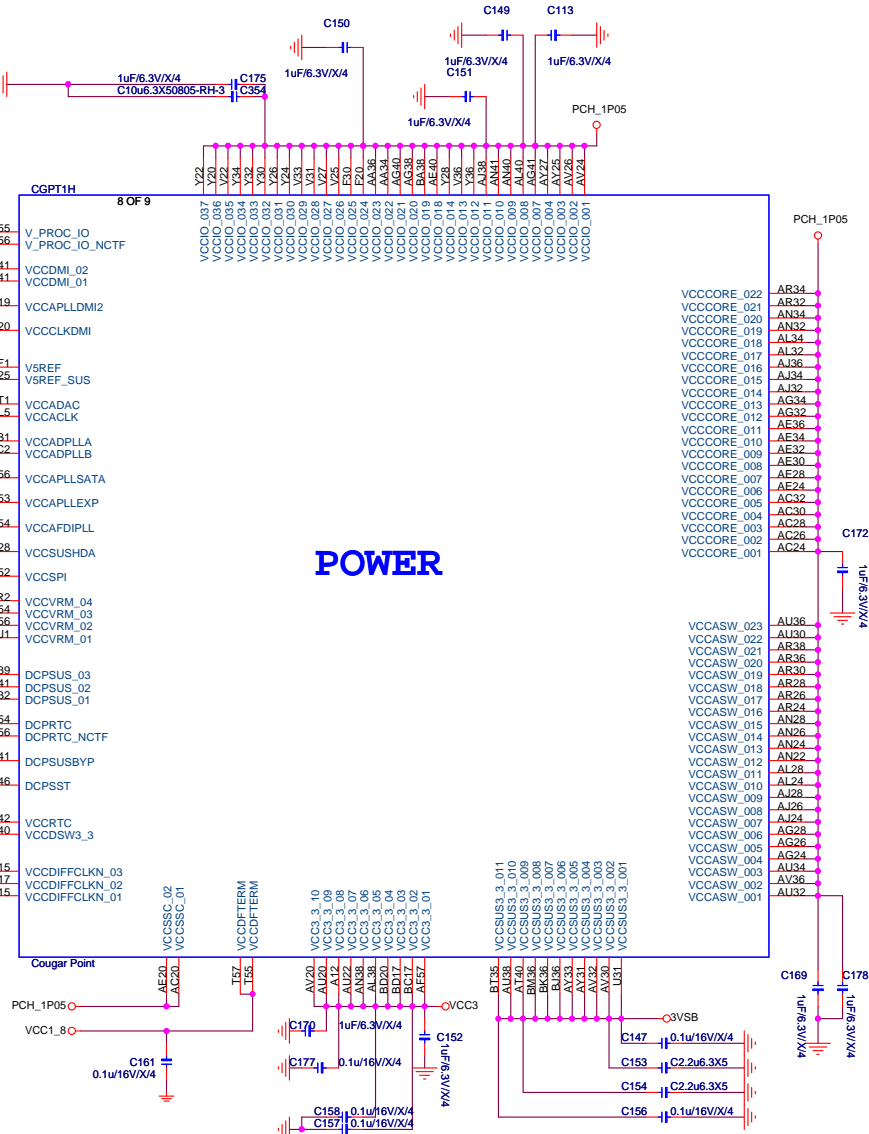
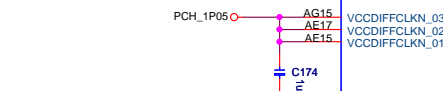
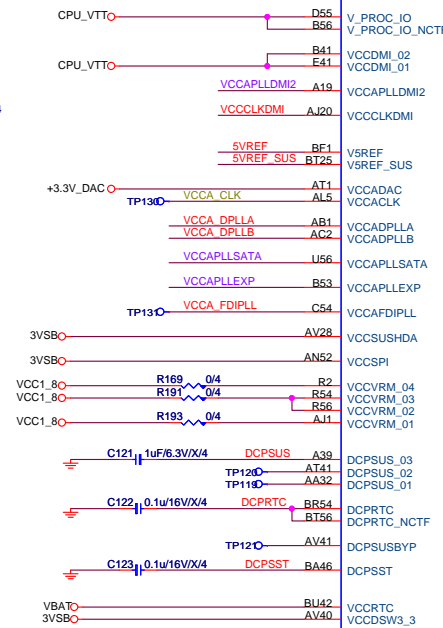
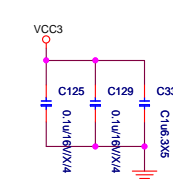
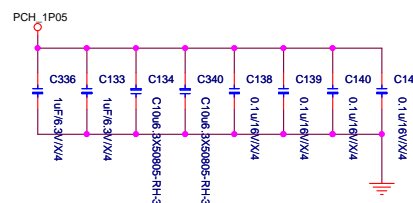
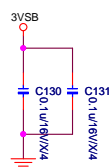
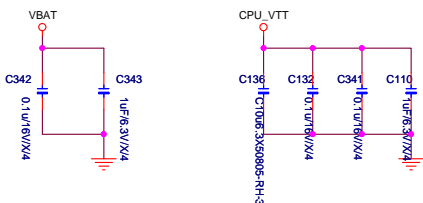
Size	Document Description	Rev
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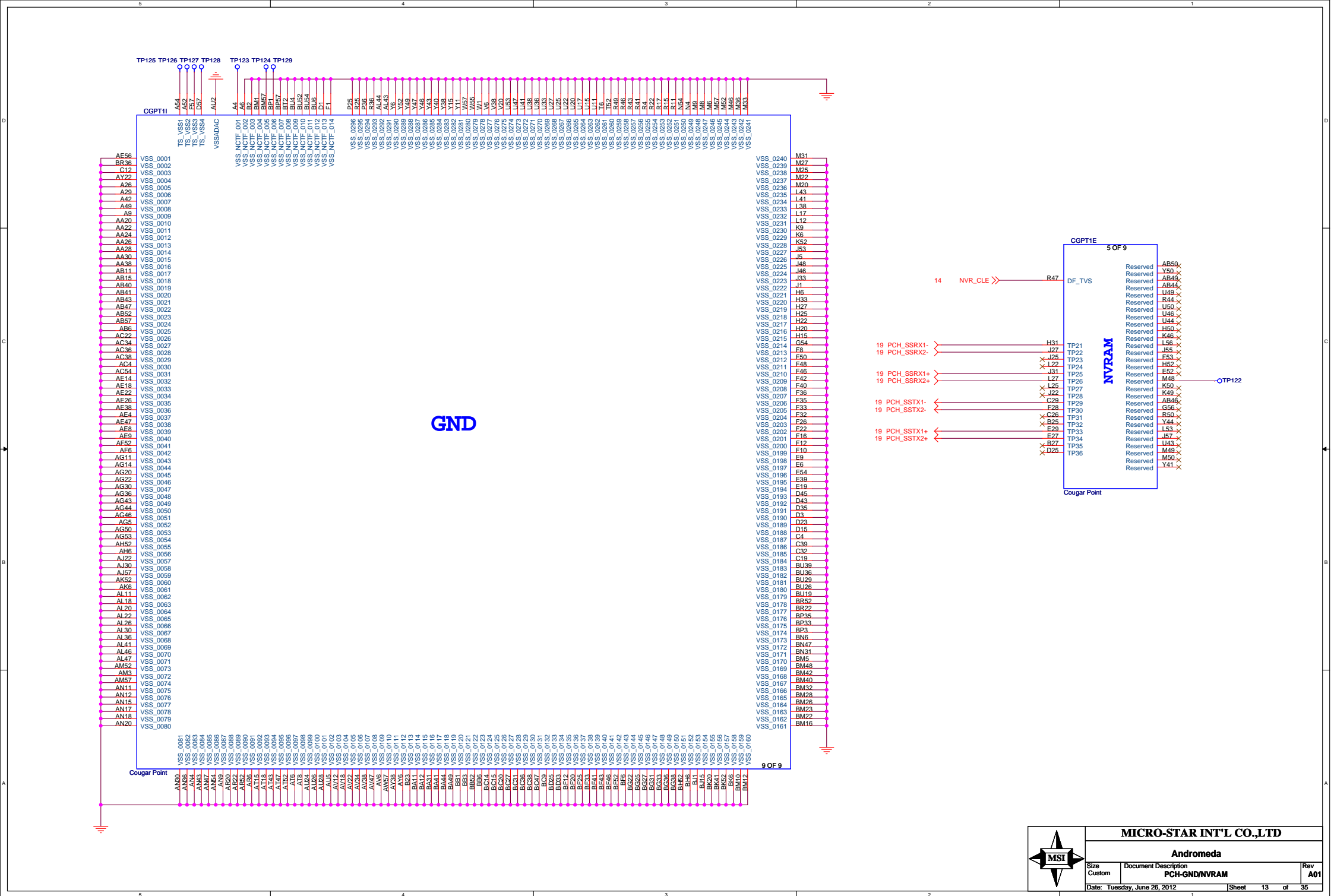
5VREF & 5VREF_SUS Sequencing Circuit



PCH decoupling cap



POWER

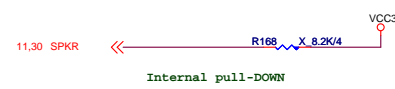
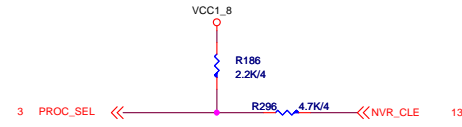
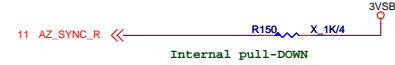
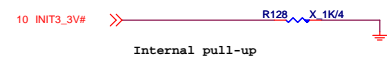
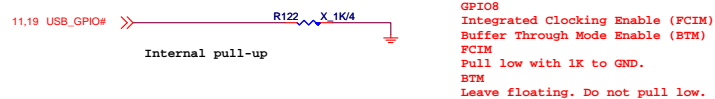
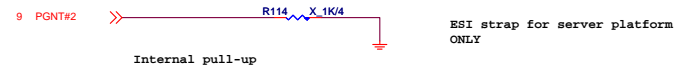
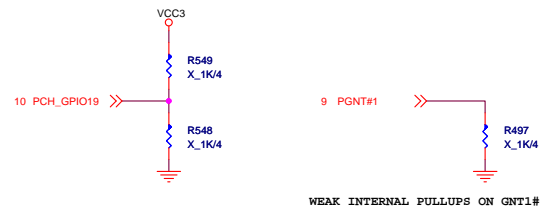


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BOOT DEVICE	GNT1	SATA1GP/GPIO19
LPC	0	0
PCI	0	0
SPI	1	1



INTVRMEN
0: DISABLE INTERNAL VRM
1: ENABLE INTERNAL VRM *

When these voltage regulators are enabled, the integrated GbE only operates at 10/100 Mbps during S3-S5.

DSWVRMEN
0: Disable Internal Deep Sleep 1.05 V regulators.
1: Enable Internal Deep Sleep 1.05 V regulators.

This signal enables the internal Deep Sleep 1.05 V regulators. Must be connected even when not supporting DSW.

HDA_SYNC
On die PLL VR volatge selector

GPIO15
Default (Disable TLS):
Leave NC. Internal pull down.

DMI/FDI TERMINATION VOLTAGE
AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP
DC COUPLED: TX/RX TO VSS IF SAMPLED LOW
DC COUPLED: TX/RX TO VCC ISF SAMPLED HIGH

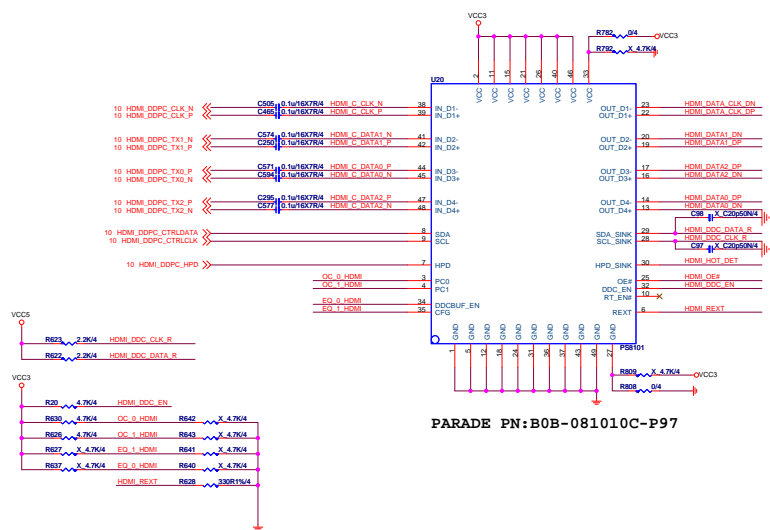
No Reboot Mode with TCO Disabled:
Connect to Vcc3_3 with 8.2k-10k Ohm weak pullup resistor.



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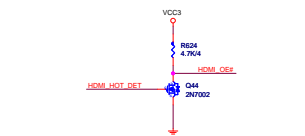
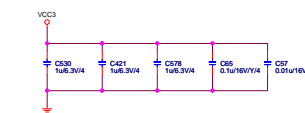
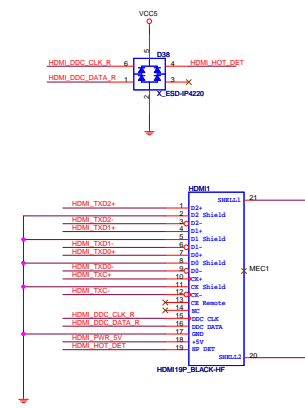
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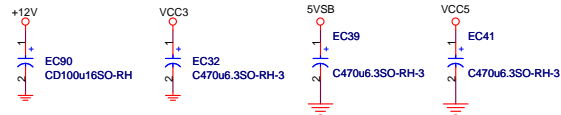
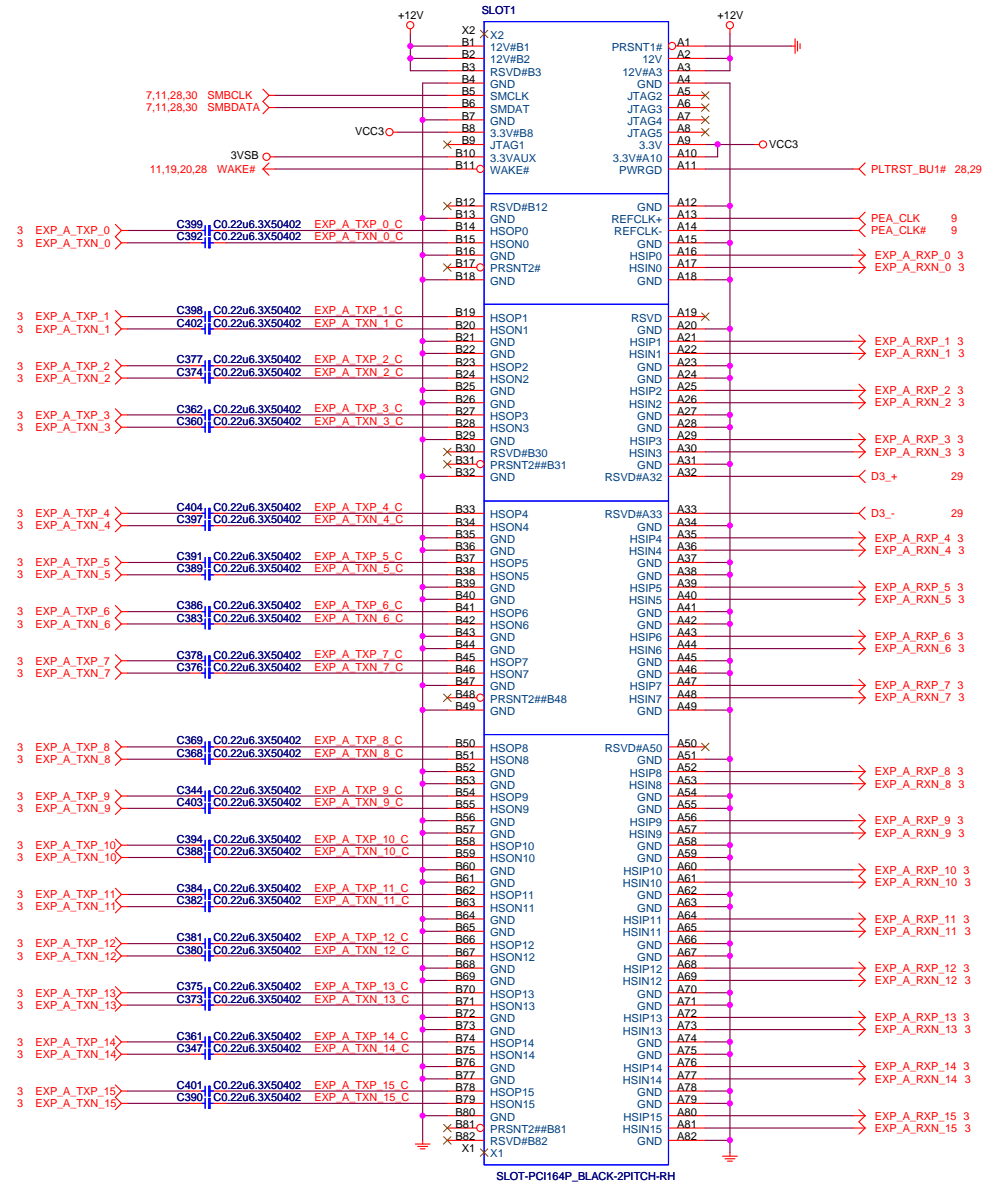


PARADE PN:B0B-081010C-P97

	"0"	"1"	note
DDC_EN	DDC level shifter disable	DDC level shifter enable	internal pull-up at ~500K ohm.
RT_EN#	input 50 ohm termination resistor enable	the input termination resistors are set to high impedances	internal pull-down at ~500K ohm.
OE#	enable	the chip is power down and input termination resistors will be at high impedance.	internal pull-down at ~500K ohm.
HPD_SINK	disable	enable	internal pull-down at ~200K ohm.
DDCBUF_EN	For DDC level shifting configuration, please refer to Table.		5V tolerant internal pull-down at ~500K ohm.
REXT			ohm. analog current generator.
DDC_EN, DDCBUF_EN, OE#	DDC Passive Switch	DDC Active Buffer	
1, 0, X	On	Off	
1, 1, 0	Off	On	
1, 1, 1	Off	Off	
0, X, X	Off	Off	
PC1, PC0			note
00	8 dB		internal pull-down at ~500K ohm.
01	4 dB		
10	12 dB		
11	0 dB		

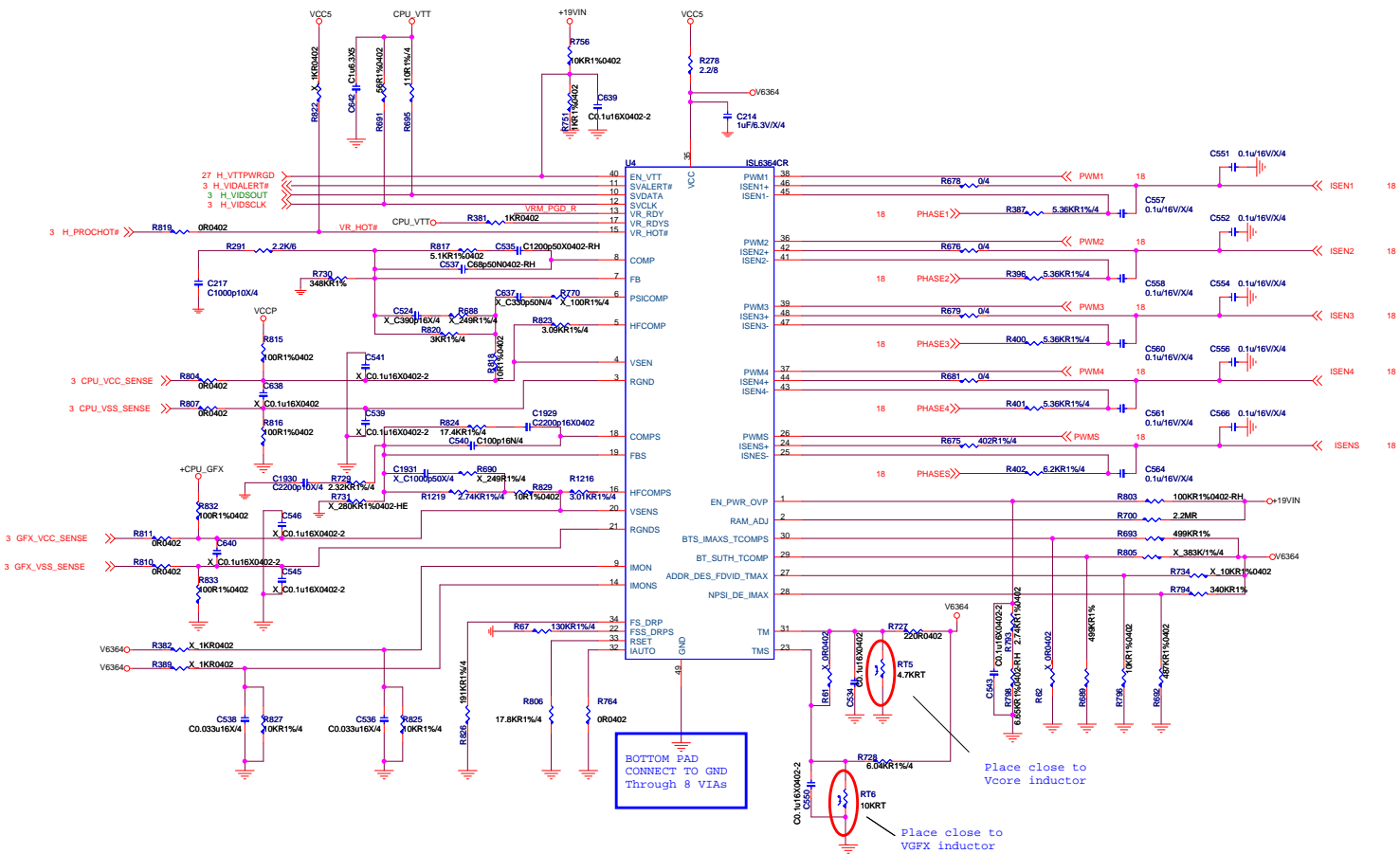


PCI EXPRESS X16 SLOT

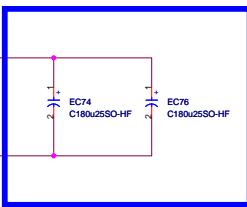
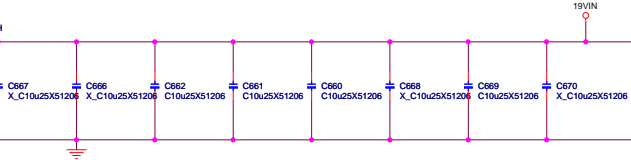
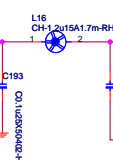
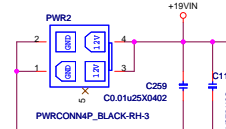
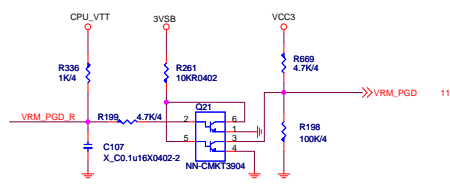


			MICRO-STAR INT'L CO.,LTD	
			Andromeda	
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VOLTAGE REGULATOR MODULE (VRD12)



VRMPWRGD LEVEL SHIFT

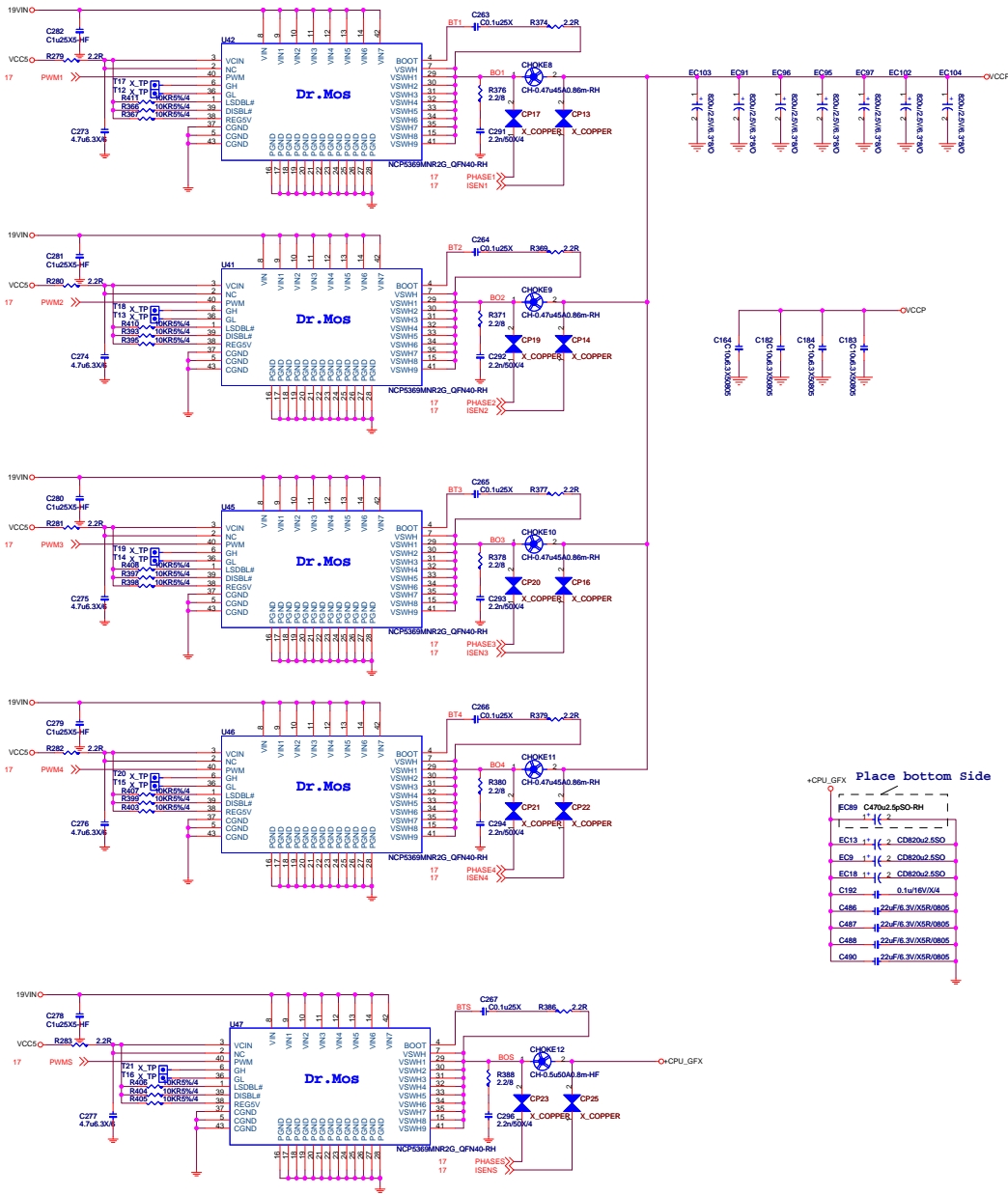


MICRO-STAR INT'L CO.,LTD

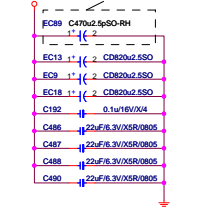
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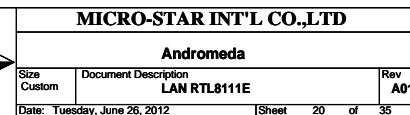
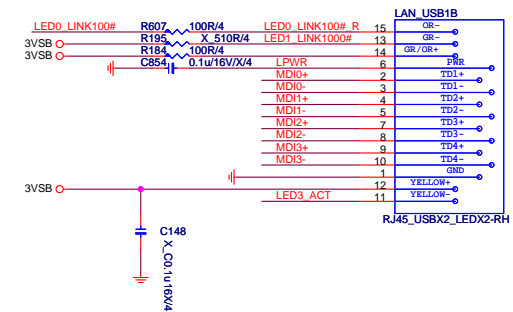
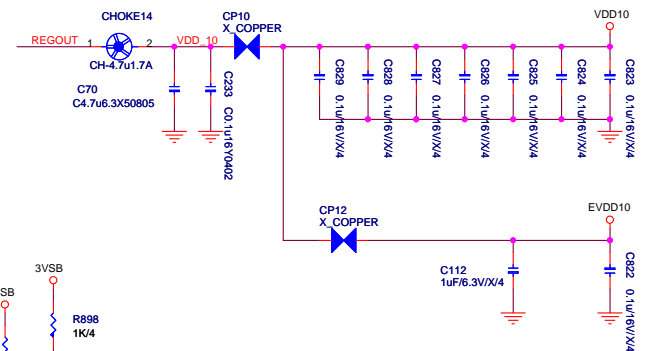
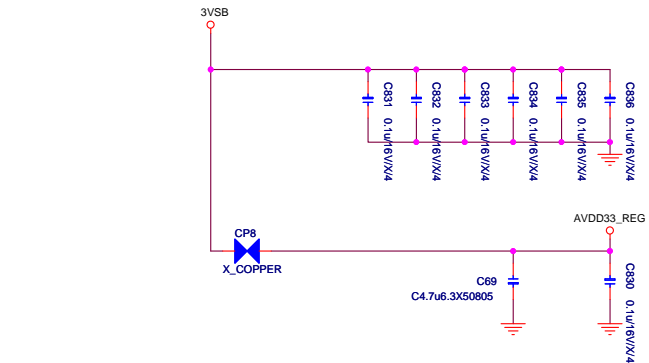
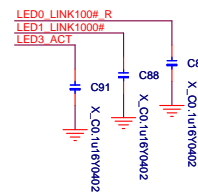
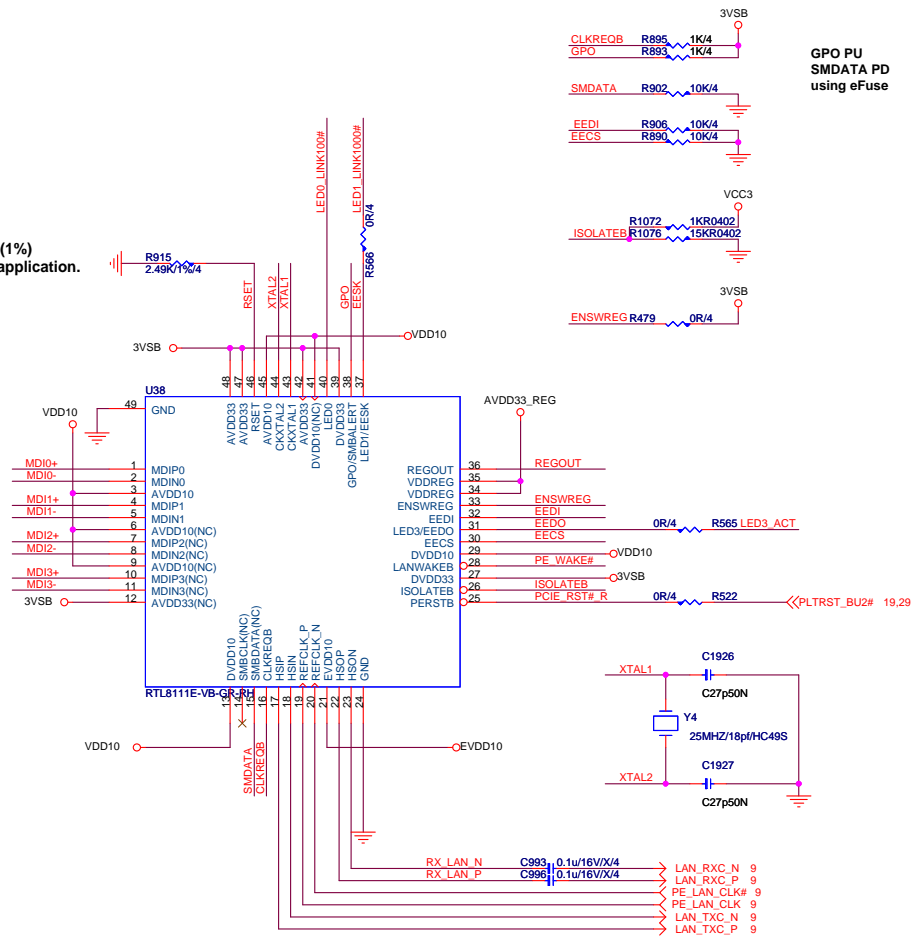
+CPU_GFX Place bottom Side

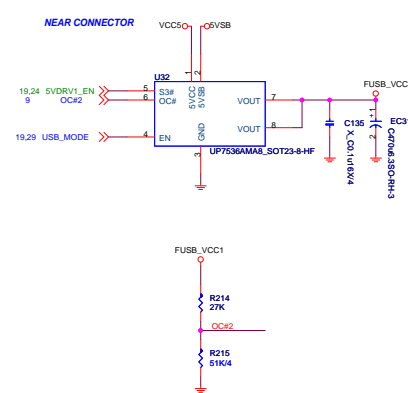
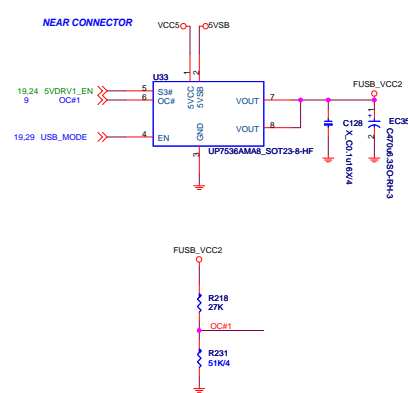
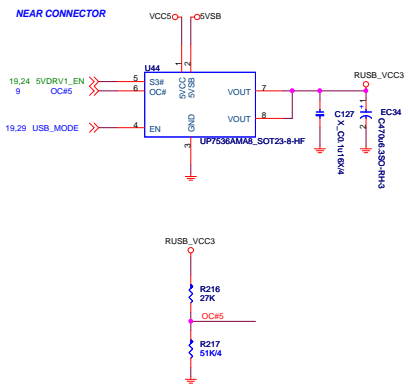
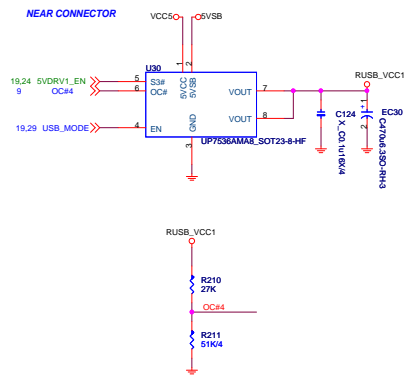


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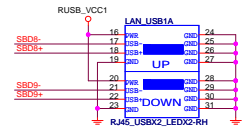
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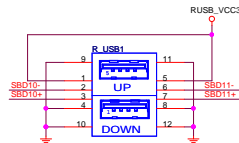




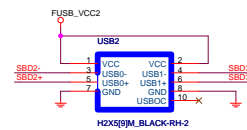
REAR USB PORT 6,7



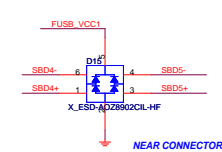
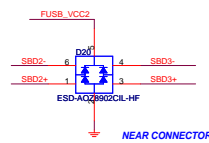
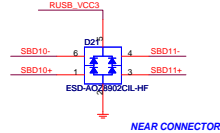
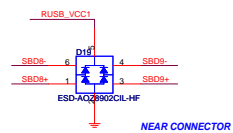
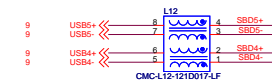
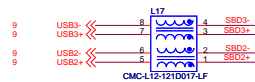
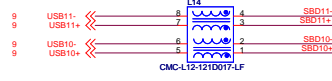
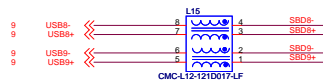
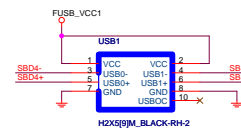
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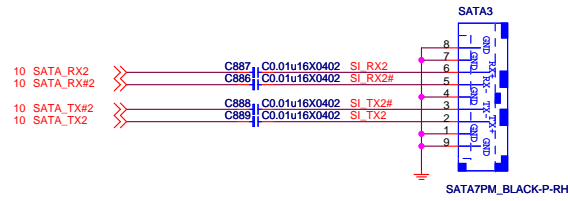
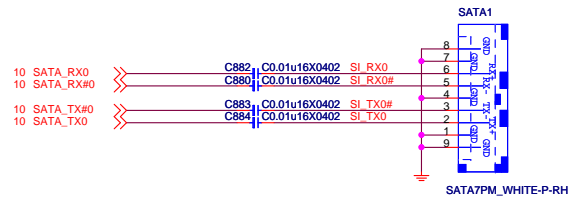


Front USB PORT 2,3

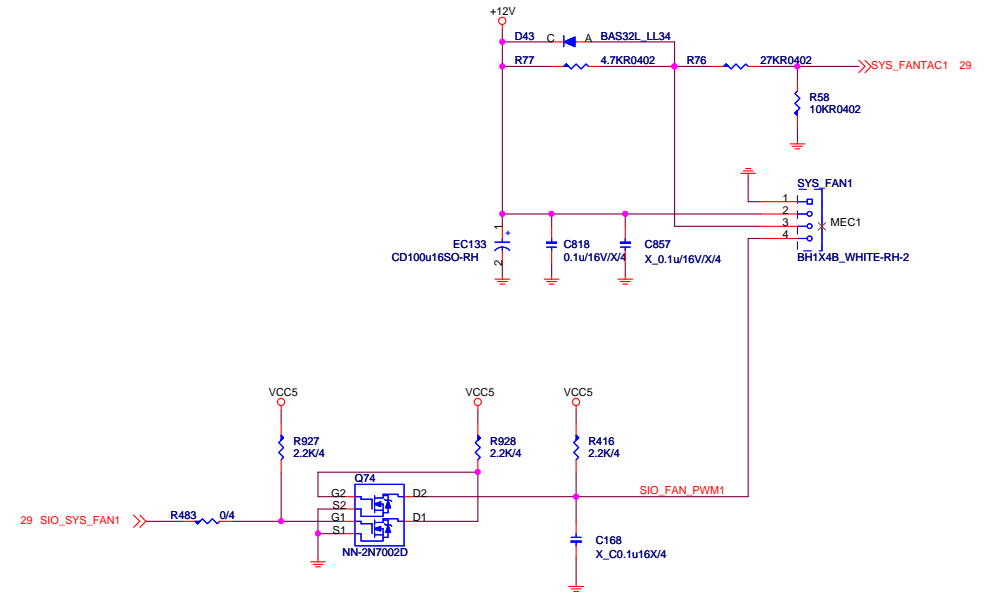


Front USB PORT 4,5

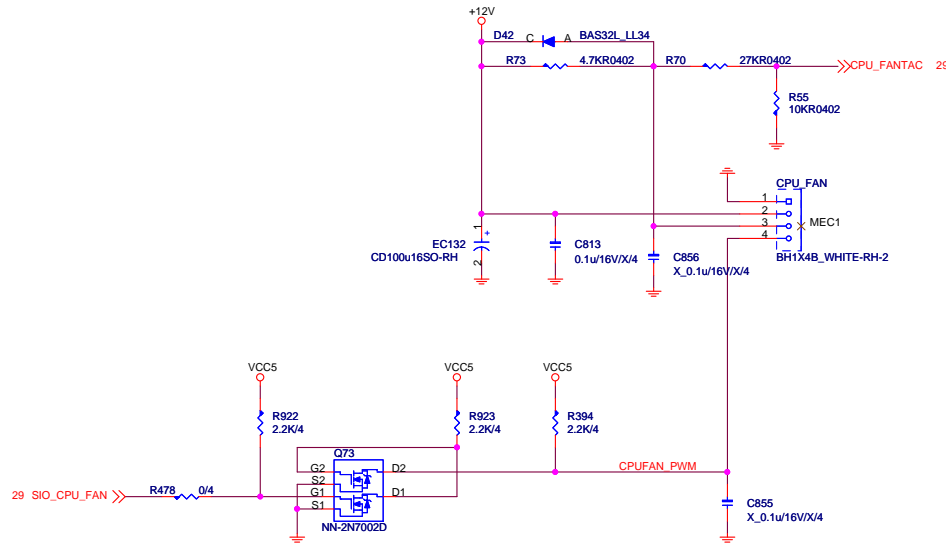




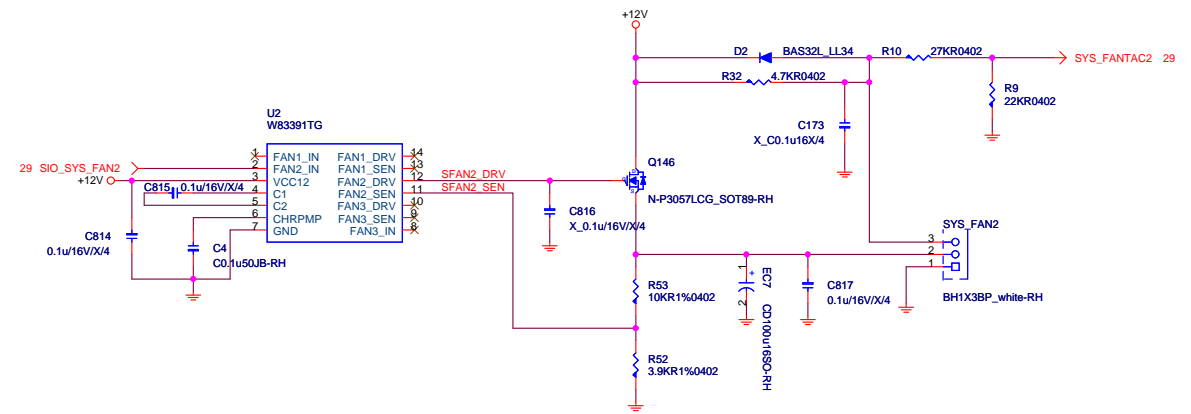
SYS Fan 1



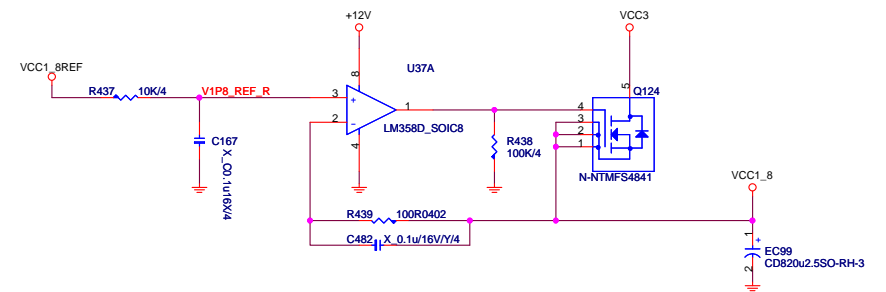
CPU Fan



SYS Fan 2

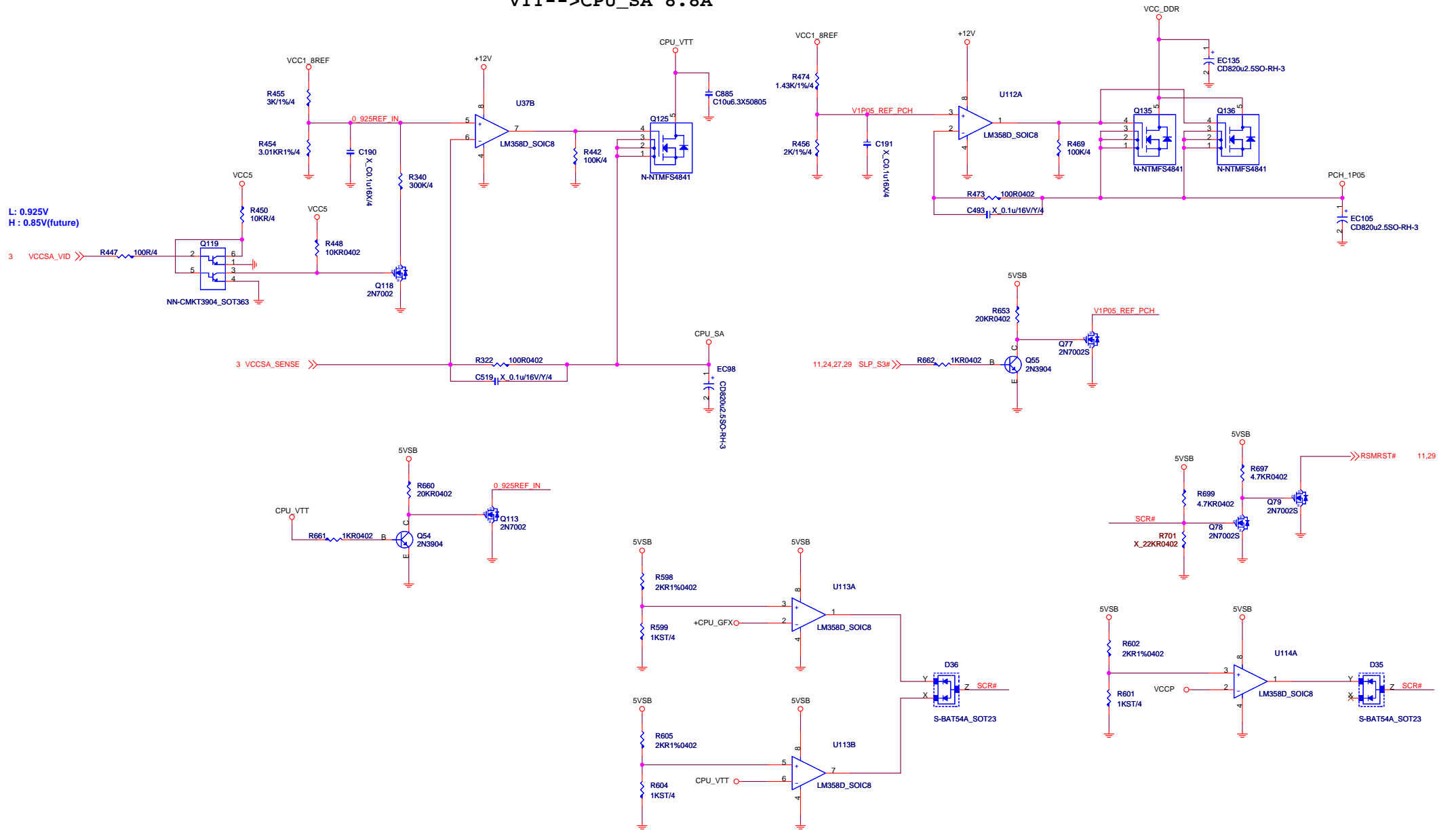


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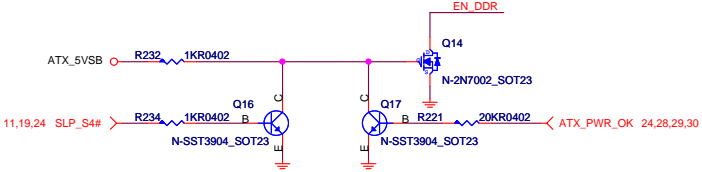
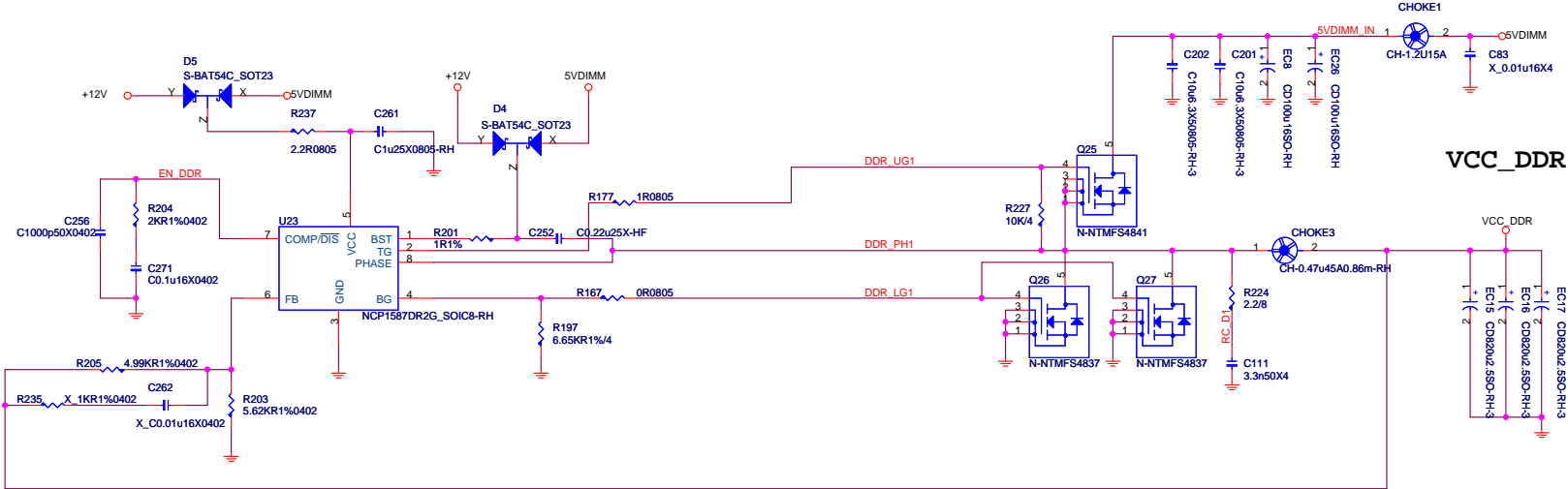


VTT-->CPU_SA 8.8A

DDR-->PCH 6.2A

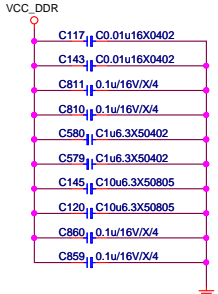
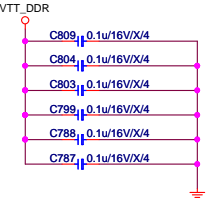
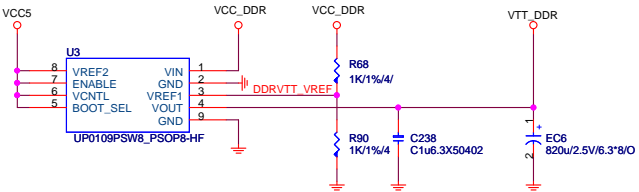


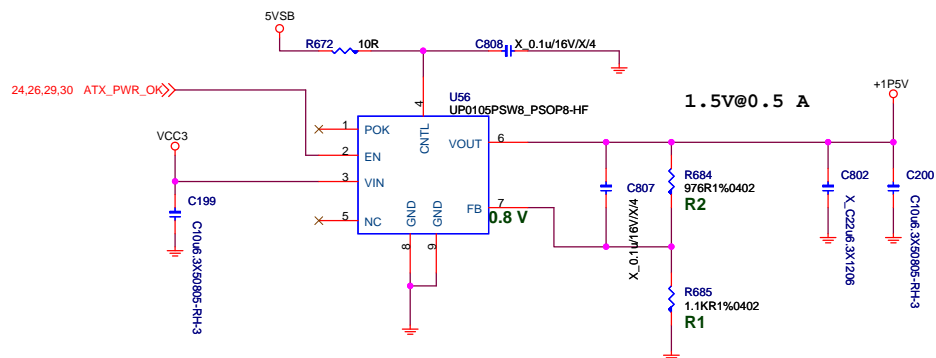
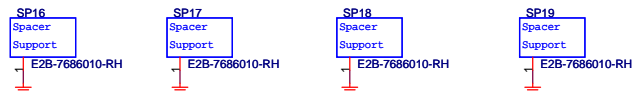
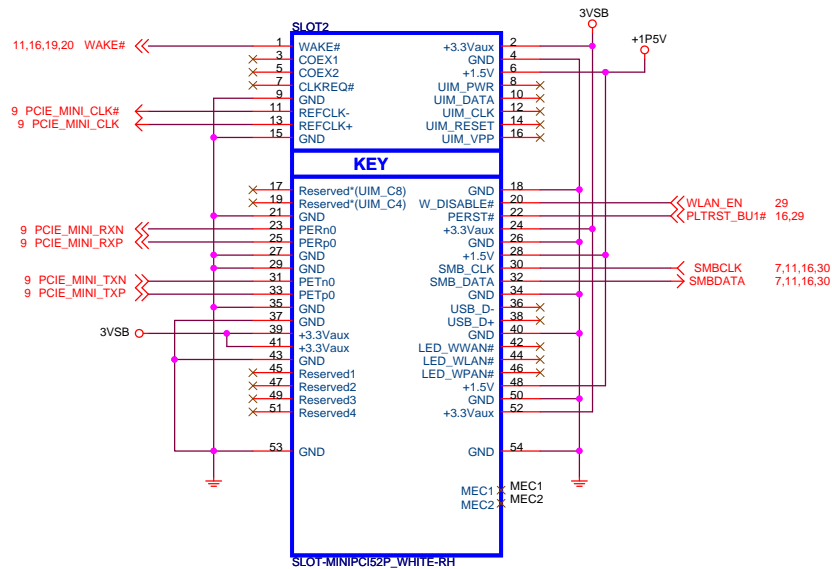
DDR III 1.5V POWER



DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .





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Size Custom

Document Description Mini slot

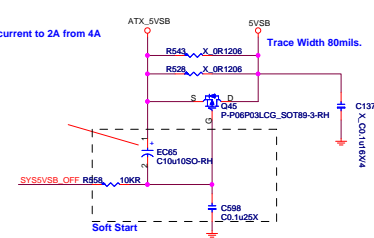
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5VSB Power Switch

Tune 5VSB inrush current to 2A from 4A



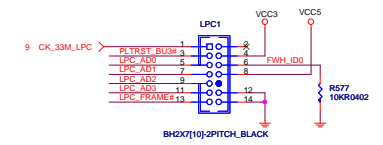
PASSWORD DETECTION

CLEAR PASSWORD JUMPER
PASSWORD Clear Password

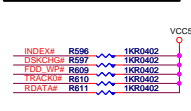


PAS_DET#
H: Did not reset password
L: Reset password

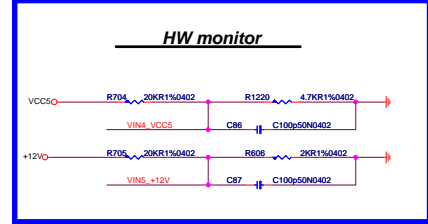
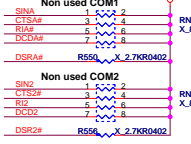
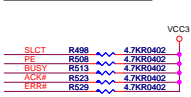
Debug Port



FLOPPY CONNECTOR



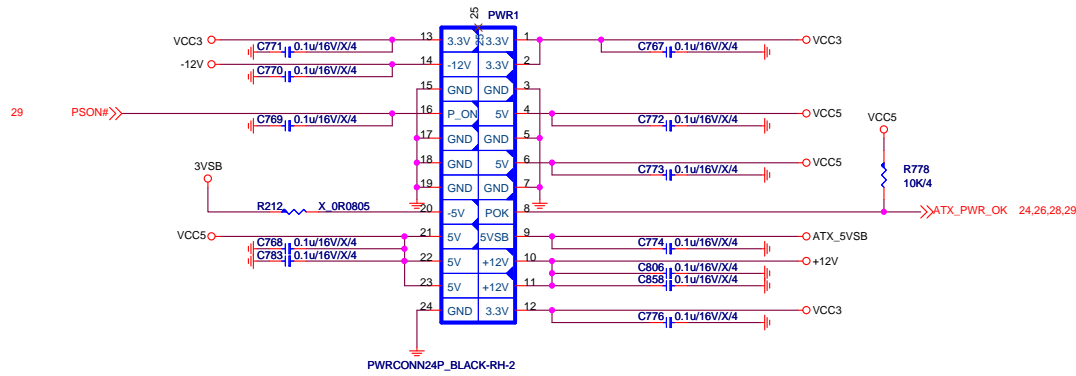
LPT CONNECTOR



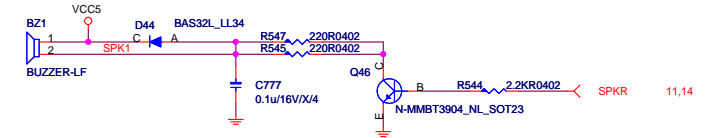
Power On Strapping Table

Symbol	Value	Description
DTRB#	1	Pin 51-56 are GPIO pins
DTRB#	0	Pin 51-56 are Bus Interface functions
RTSB#	1	Fan control mode: PWM mode.
RTSB#	0	Fan control mode: DAC mode.
SLIN#	PU-1k	Pin 100-116 as LPT1 interfaces
SLIN#	PU-20k	Pin 100-116 as PVID Controller
PD-1k	Pin 102/103/111/112 as SVID Controller	
PD-47k	Pin 100-103 and pin 105-116 as GPIO pins	
DTRA#	1	Fan full duty is 60%.
DTRA#	0	Fan full duty is 100%.
RTSA#	1	Enable the 80 port function.
RTSA#	0	Disable the 80 port function.
SOUTA	1	Configuration Register IO port is 4E4F.
SOUTA	0	Configuration Register IO port is 2E2F.
SOUT2	1	OVP warning mode
SOUT2	0	OVP force mode

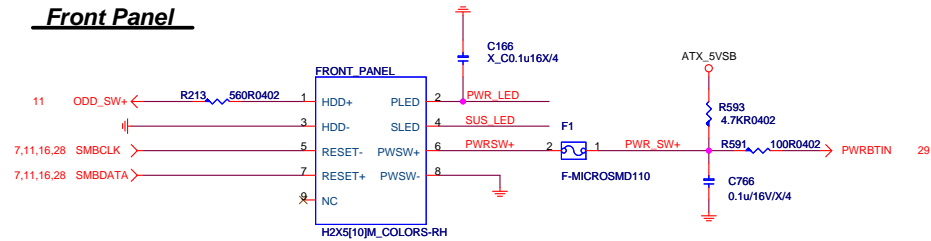
ATX POWER CONNECTOR



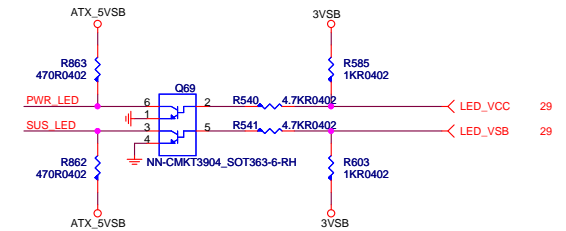
Buzzer Circuit



Front Panel



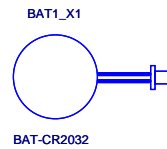
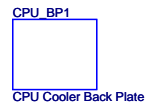
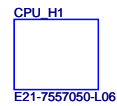
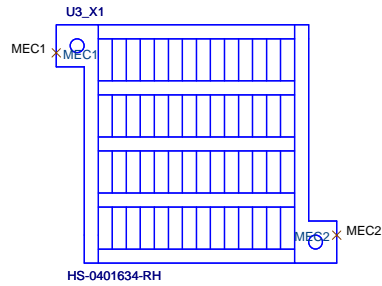
Power LED



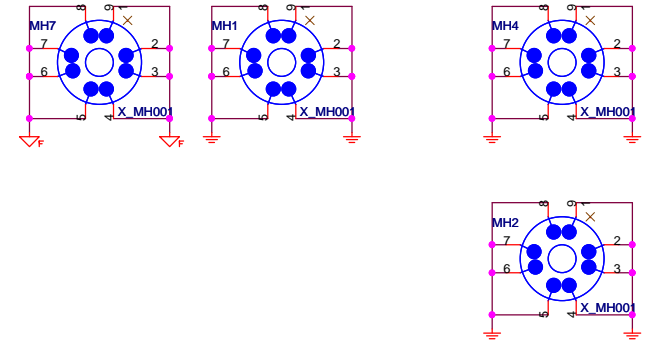
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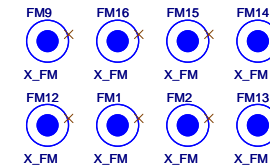
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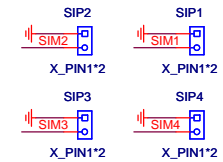
Mounting Holes



Optical Fiducial Marks-120



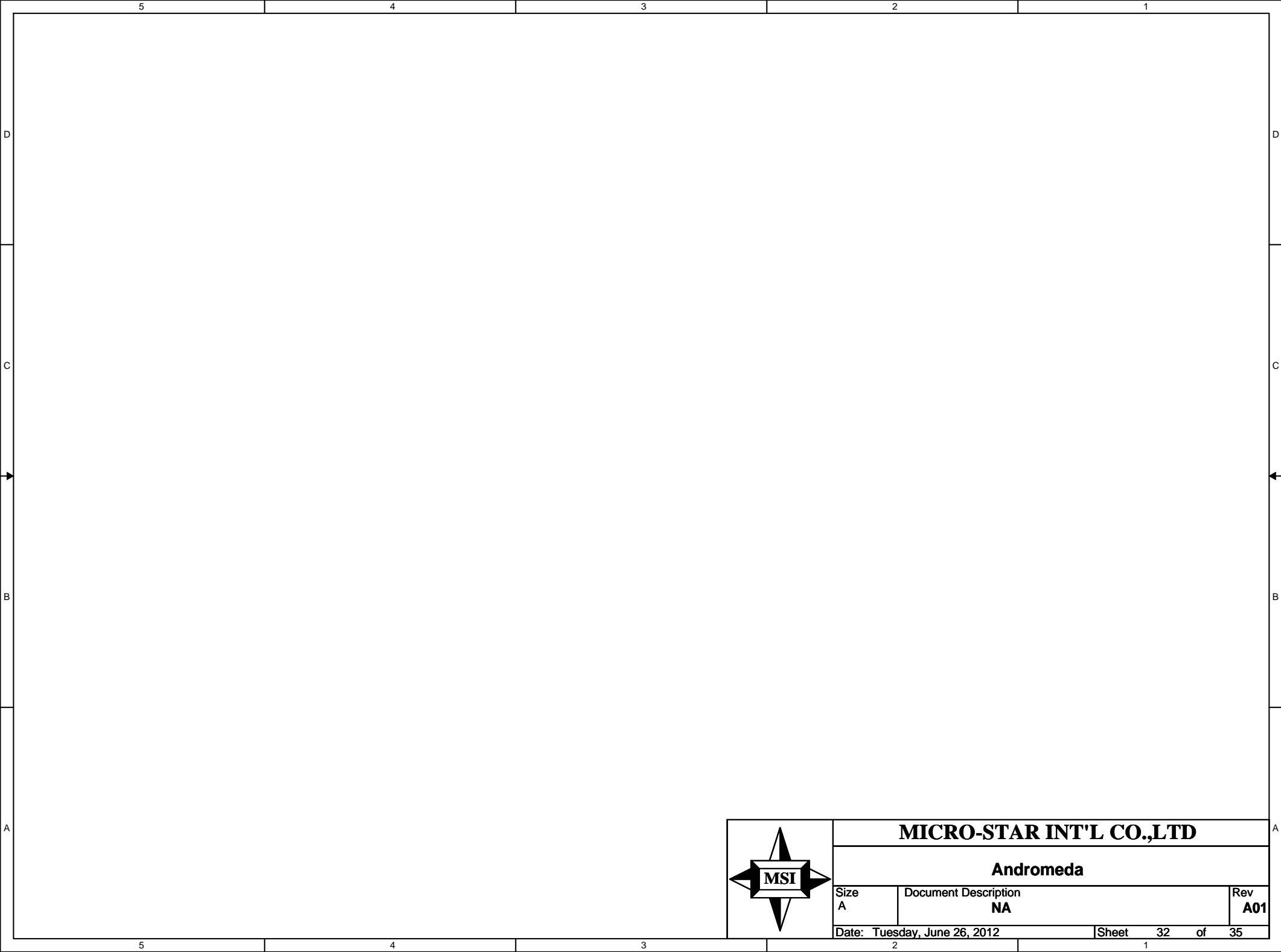
Simulation



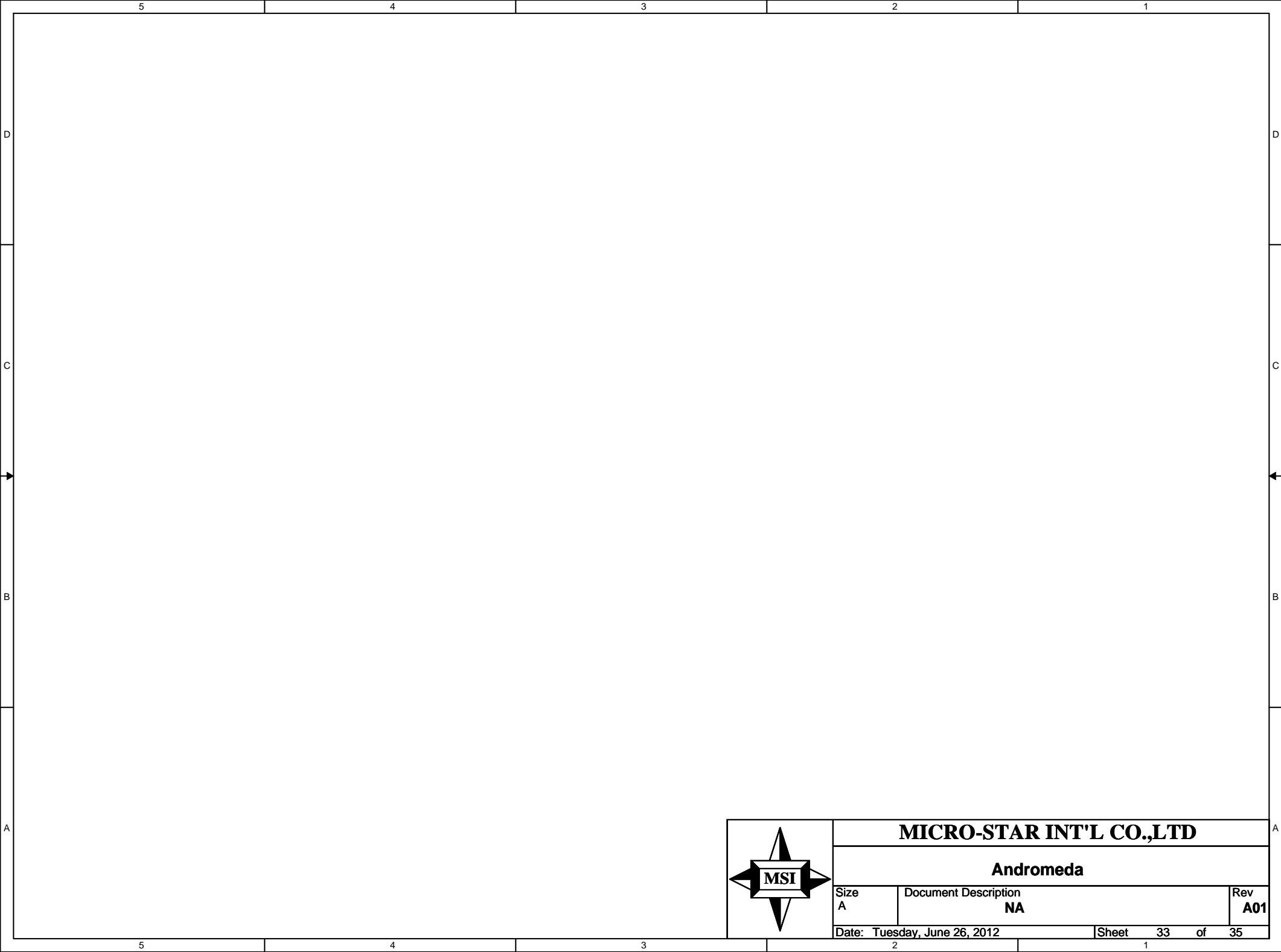
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Andromeda			
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